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PATENT
30205/38071A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Jae Jin Lee

Serial No.: 10/755,732

Filed: January 12, 2004

For: Signal Delay Control Circuit in a Semiconductor Memory Device

Group Art Unit: 2818

Examiner: Ly D. Pham

I hereby certify that this paper and the documents referred to as enclosed therewith are being deposited with the United States Postal Service as first class mail, postage prepaid, on **September 30, 2004**, in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450

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COMMENT ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In addition to the reasons for allowance set forth in the allowance papers that were mailed in connection with the present application, it is respectfully submitted that the claims are allowable for the additional reasons that the invention defined by the language of the claims is neither anticipated by, nor would have been obvious when taken as a whole in view of, the art of record.

Respectfully submitted,

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September 30, 2004 By:

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